**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended) A method of manufacturing an insulated gate field effect transistor; including:

providing a substrate having a first major surface having a low-doped region at the first major surface, the low-doped region having a concentration of less than $5x10^{14}$ $cm^{-3}$ at the first major surface;

forming gate trenches extending from the first major surface;

forming trench insulator on ~~the~~ a base and sidewalls of the gate trenches;

implanting dopants of a first conductivity type at the base of the trenches;

implanting a body implant of second conductivity type opposite to the first conductivity type in the low-doped regions between the gate trenches;

carrying out a diffusion step to form an insulated gate transistor structure in which the body implant diffuses towards the substrate in the ~~low-doped~~ low-doped region to form a p-n junction between a body region doped to have the second conductivity type above a drain region doped to have the first conductivity type, the p-n junction being deeper below the first major surface between the trenches than at the gate trenches; and

forming source regions at the first major surface adjacent to the gate trench.

2. (currently amended) A method according to claim 1 in which the p-n junction boundary between drain and body region is deeper between the gate trenches than the depth of the trenches.

3. (currently amended) A method according claim 1 in which the insulated gate field effect transistor structure formed in the diffusion step has an additionally doped region of

first conductivity type at the base of the gate trenches having a doping density below $5x10^{16}$ $cm^{-3}$ but higher than in the drain regions between the gate trenches.

4. (previously presented) A method according claim 1, wherein the step of implanting a body implant implants the body implant has a dose of at most $5x10^{13}$ $cm^{-2}$.

5. (currently amended) A method according to claim 1 further comprising the step of,

forming a pattern laterally across the first major surface of the substrate, the pattern doped to have lower-doped regions of first conductivity type alternating with higher-doped regions of first conductivity type, wherein the lower-doped regions have a concentration of less than about $5x10^{14}$ $cm^{-3}$ and, the higher-doped regions have a concentration between about $1x10^{16}$ $cm^{-3}$ and $3x10^{16}$ $cm^{-3}$;

wherein the gate trenches ~~(10)~~ are formed in the higher-doped regions.

6. (currently amended) A method according to claim 5 wherein:

the step of forming a pattern laterally across the first major surface of the substrate includes:

depositing an epilayer of semiconductor doped to have a lower doping density;

patterning a plurality of trench etch windows spaced laterally across the substrate; and

implanting dopants though the trench etch windows, the dopants being of a first conductivity type;

wherein the step of forming gate trenches in the ~~higher-doped~~ higher-doped regions includes etching gate trenches through the trench etch windows.

7. (original) A method according to claim 5 wherein the step of forming a pattern laterally across the first major surface of the substrate includes:

etching a plurality of semiconductor trenches spaced laterally across the substrate in a layer of lower doping density; and

growing semiconductor doped to have a higher doping density in the semiconductor trenches.

8. (currently amended) A method according to ~~claim 1,~~ claim 7, wherein the semiconductor is silicon and the first conductivity type is n-type.

9. (currently amended) A method according to claim 1, for making an insulating gate field effect transistor of predetermined breakdown voltage for which the doping of ~~a~~ an epilayer for forming ~~a conventional~~ an insulated gate field effect transistor without the step of implanting dopant at the gate of the gate trench has a first predetermined doping concentration;

wherein the doping of the ~~low-doped~~ low-doped region at the first major surface is at most one half of the predetermined doping concentration.

10. (currently amended) A method according to claim 1, further comprising performing a moat etch by etching the first major surface to form ~~semiconductor away from~~ the gate trenches to a depth below the bottom of the source region.

11. (previously presented) A trench FET formed by the method of claim 1.